CLAIMS

1. A method of forming a semiconductor device fuse, the method comprising:

depositing a first passivation layer on a patterned top-most metal layer in a semiconductor device;

patterning and etching the first passivation layer to provide access to at least two fuse contacts located in the top-most metal layer;

depositing a conductive pad metal layer on the patterned first passivation layer;

patterning and etching the conductive pad metal layer to form a metal fuse region connecting the at least two fuse contacts; and

depositing a second passivation layer on the patterned conductive layer.

2. The method as recited in claim 1 wherein the first passivation layer is further patterned to form a first pad opening in the first passivation layer.

3. The method as recited in claim 2 wherein the conductive pad metal layer is further patterned to form a metal pad over the first pad opening in the first passivation layer.

4. The method as recited in claim 1 further comprising patterning the second passivation layer to form a second pad opening.

5. The method as recited in claim 1 further comprising patterning the second passivation to form a second pad opening and a partially etched region over the metal fuse region.

6. The method as recited in claim 1 further comprising depositing a barrier layer prior to depositing the conductive pad metal layer on the patterned first passivation layer.

7. The method as recited in claim 6 wherein the barrier layer comprises one of tantalum and tantalum nitride.

8. The method as recited in claim 1 wherein the thickness of the deposited second passivation layer is selected so that the reflectivity of the passivation layer over the area of the fuse is minimized.

9. The method as recited in claim 1 further comprising partially etching the second passivation layer over the area of the fuse to be blown to reduce the reflectivity of the passivation layer over the area of the fuse to be blown.

10. The method as recited in claim 1 wherein the conductive pad metal layer comprises aluminum.

11. The method as recited in claim 1 wherein the top-most metal layer comprises copper.

12. The method as recited in claim 1 wherein a portion of the metal fuse region is formed on a portion of the patterned first passivation layer.

13. The method as recited in claim 1 wherein the first passivation layer is comprised of one of silicon dioxide and silicon nitride.

14. The method as recited in claim 1 wherein the first passivation layer is comprised of a combination of layers comprising at least one of silicon dioxide and silicon nitride.

15. The method as recited in claim 1 wherein the second passivation layer is comprised of one of silicon dioxide and silicon nitride.

16. A semiconductor device having a fuse comprising:

a first dielectric layer disposed on top of a top copper interconnect layer of a semiconductor device, said dielectric layer having at least one opening providing access to at least two fuse contacts;

a pad metal layer disposed on the patterned first dielectric layer, said pad metal layer forming a fuse connecting the at least two fuse contacts; and

a second dielectric layer disposed on at least a portion of the fuse material in the pad metal layer.

17. The semiconductor device of claim 16 wherein the pad metal layer comprises aluminum.

18. The semiconductor device of claim 16 wherein the pad metal layer is further patterned to form a pad for connecting to an external circuit.

19. The semiconductor device of claim 18 wherein the second dielectric layer is patterned to form a pad opening over the pad.

20. The semiconductor device of claim 16 wherein the second dielectric layer is a conformal layer having a thickness selected so that the reflectivity of the dielectric layer over the area of the fuse to be blown is minimized.

21. The semiconductor device of claim 16 wherein the second dielectric layer over the area of the fuse to be blown has a thickness selected so that the reflectivity of the dielectric layer over the area of the fuse to be blown is minimized.